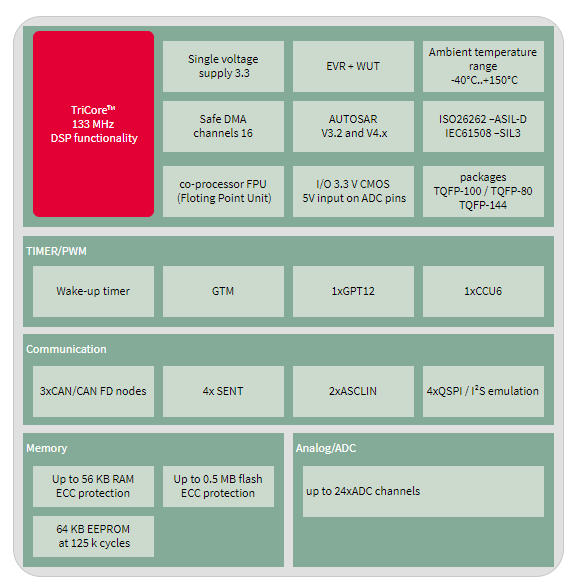
**LV DC Controller Study**

**SAK-TC213L-8F133F AC**

****

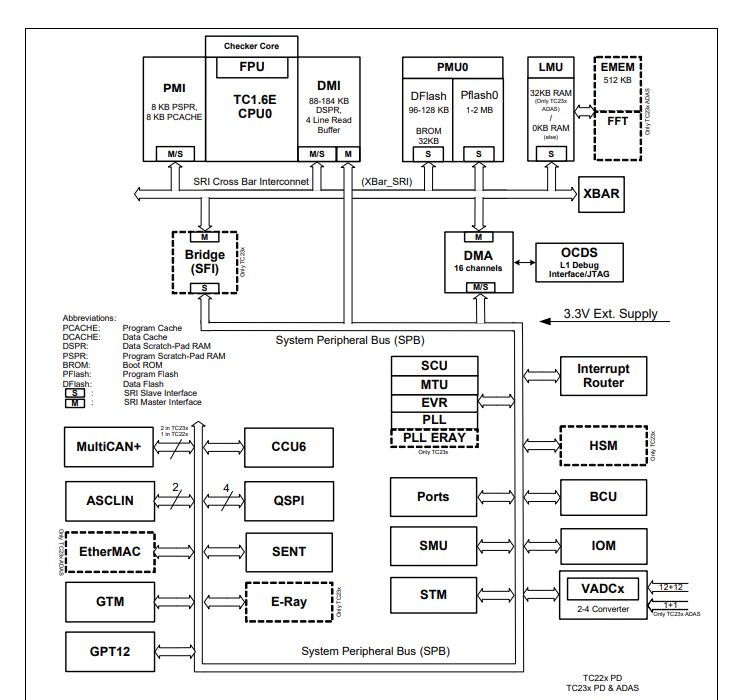
Clock Frequency: 133MHz

1 core with FPU

Tricore means with RISC, DSP, MCU functionality in a single core doesn’t imply all Tricores are with 3 Independent cores.

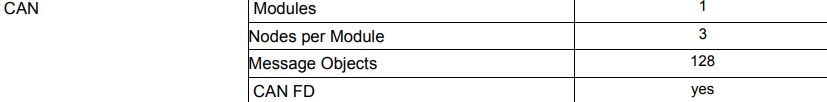
IO Operation Voltage 3.3V, 5V supported in ADC Pins

Up to ASIL D and ISO 26262 Compliant



**On Chip Peripherals**

**CAN Module**

****

Debug over CAN possible

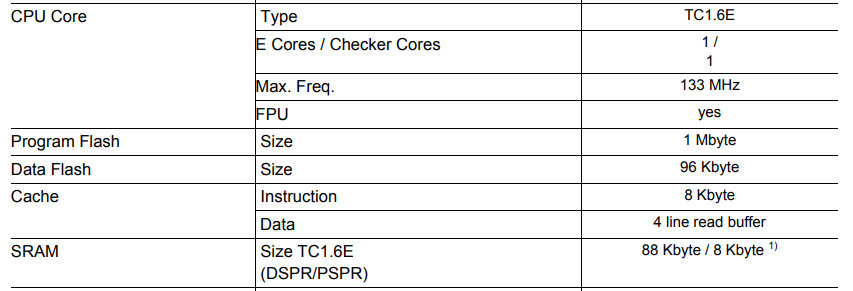
**3** independently operating CAN nodes with Full-CAN functionality

CAN FD functionality is available on all nodes of module.

3 Nodes with a total of 128 message objects

3 channels and ports can be configured for each nodes

**Memory**



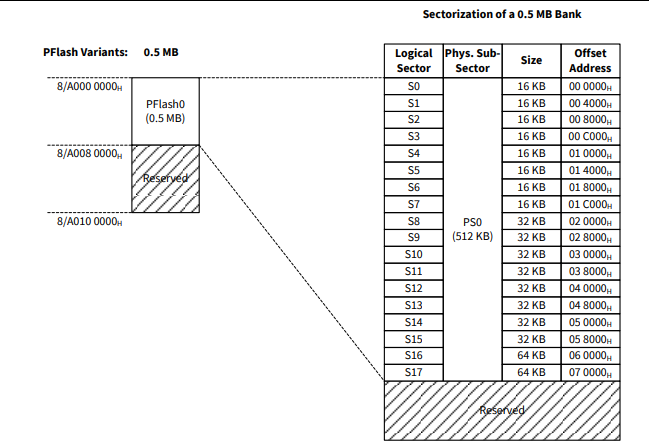
P Flash: 0.5Mb

D flash: 64Kb

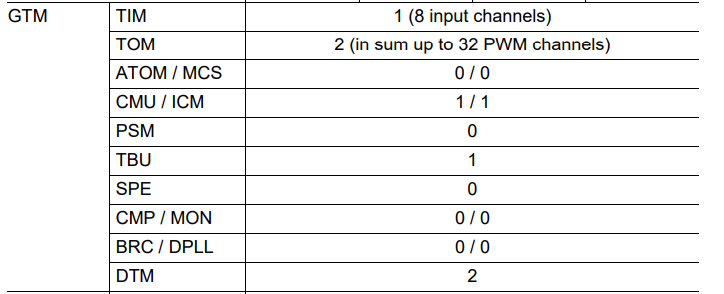
SRAM : 56KB inc. Cache

Core 0 : DSPR 48KB PSPR 8KB

16 DMA Channels



**Generic Timer Module**



TIM (Timer Input Module) is having PWM Measurement mode – Can be used to measure the Duty cycle, Period of the incoming PWM

TOM (Timer Output Module) – 16 Independent channels to generate simple **PWM**

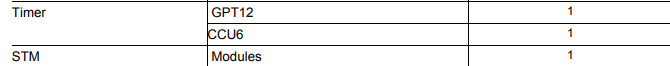
**CCU6 Capture / Compare Unit**

Timer T12 Block with three capture/compare channels and a Timer T13 Block with one compare channel.

T12 can independently generate 3 phase PWM both center and edge aligned -25.2 section

T13 can be used to generate Single Channel PWM

**GPT for PWM**

****

**ADC based on SAR**

****

2 Independent ADC Modules (12+12 Channels)

12 Channel ADC each i.e. 24 input Lines

Input Voltage 0 to 5.5V (ADC supply)

Resolution 12Bits

**QSPI**

4 Queued SPI Interface Channels (QSPI) with master and slave capability up to 50 Mbit/s

**PORT - GPIO**

Digital programmable I/O ports

Port 00,02,10,11,13,14,15,20,21,22,23,33,34,40,41

**On chip debug support**

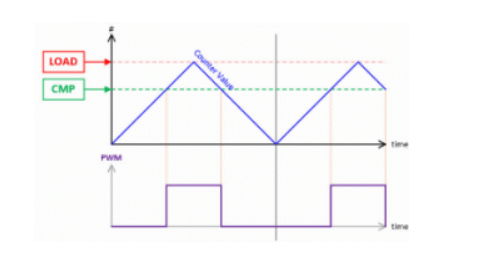
**Bus SRI SPB**

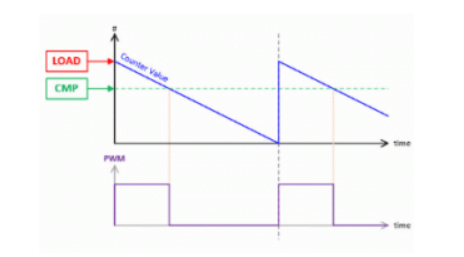
**Mem Map**

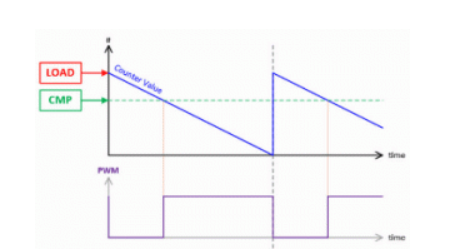
**Boot ROM**

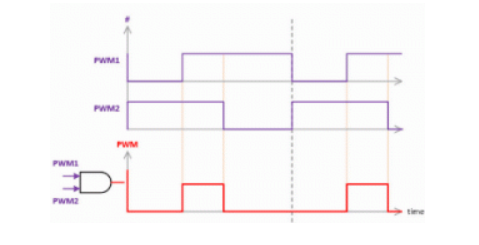
**System Timer**

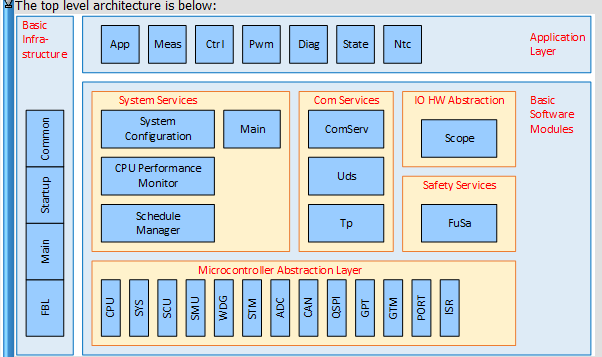
**PWM Generation in General**











APPLICATION LAYER

**Hsfb APP** is a component in Application layer of the LV DCDC

Top layer has 1 init schedule

5 periodic schedules 30 30 100 micro 1 10 milli secs

All other components in appl layer is called by this component Hsfb APP